Amendments to the Claims:

1. (Currently Amended) A method for use in connection with an integrated circuit design, the method comprising:

identifying distinct timing paths of the integrated circuit design, the distinct timing paths having timing violations;

~~associating a first plurality of the distinct timing paths with a first set of timing paths, individual ones of the first plurality belonging to a second set of timing paths and including a first common characteristic; and~~

~~improving the first set of timing paths based on at least in part on an improvement to an individual timing path of the first set of timing paths.~~

identifying a first subset of the distinct timing paths including a plurality of timing paths wherein each of the plurality of timing paths includes at least one first common characteristic;

within the plurality of timing paths forming the first subset, grouping the timing paths into one or more groups, each timing path within a group having at least one second common characteristic,

correcting a first timing path violation for one of the timing paths within the group; and

repeating the first timing path violation correction for at least one of the other timing paths within the group.

2. (Currently Amended) The method, as recited in claim 1, wherein the second ~~first~~ common characteristic is a sequence of devices.

3. (Currently Amended) The method, as recited in claim 1, further comprising:

~~associating~~ identifying a second ~~plurality~~ subset of the distinct timing paths including a second plurality of timing paths ~~with the second set of timing paths~~, wherein each of the second plurality of timing paths ~~individual ones of the second plurality including a second~~ includes at least one third common characteristic; and~~, the associating based at least in part on a prioritization of individual ones of the second set of timing paths~~

wherein a particular timing path including the at least one first characteristic and the at least one third characteristic is identified with a subset based on a prioritization of the first subset and the second subset.

4. (Currently Amended) The method, as recited in claim 3, wherein the prioritization is based at least in part on the number of ~~paths included in individual ones of the second plurality of sets of timing paths~~ groups within each subset.

5. (Currently Amended) The method, as recited in claim [[3]] 1, wherein the ~~first set of timing paths is one of a first plurality of sets associated with the second set of timing paths~~ grouping further includes forming one or more other groups, each timing path within the other groups being a common portion of a timing path of the other groups, and having a common sequence of device elements.

6. (Currently Amended) The method, as recited in claim [[3]]1, wherein the first common characteristic comprises an origin of a timing path.

7. (Currently Amended) The method, as recited in claim [[3]]1, wherein the first common characteristic comprises a destination of a timing path.

8. (Currently Amended) The method, as recited in claim [[3]]1, wherein the first common characteristic comprises inclusion of a first block in a timing path.

9. (Currently Amended) The method, as recited in claim [[3]]1, wherein the first common characteristic comprises inclusion of a first net in a timing path.

10. (Currently Amended) The method, as recited in claim 1, wherein correcting a first timing path violation ~~the improvement~~ includes reducing a maximum timing violation.

11. (Currently Amended) The method, as recited in claim 1, wherein correcting a first timing path violation ~~the improvement~~ includes reducing a minimum timing violation

12. (Currently Amended) The method of claim 1, further comprising:

substituting in the integrated circuit design, a plurality of replacement circuits, each ~~individual~~ one[[s]] of the plurality of replacement circuits corresponding to a respective ~~ones of the first set of~~ timing path[[s]] of the group, the plurality of circuits based at least in part on the ~~improvement to~~ correction of the first timing path violation.

13. (Currently Amended) The method of claim 12, further comprising:
fabricating an integrated circuit including the plurality of replacement circuits.

14. (Currently Amended) The method of claim 1, further comprising:
preparing the integrated circuit design and thereafter performing the ~~improving~~ correcting and repeating.

15. (Currently Amended) A semiconductor integrated circuit manufactured using the method of claim 1. ~~comprising:~~

~~a plurality of circuits having distinct timing paths, the distinct timing paths having a first common characteristic;~~

~~wherein individual ones of the plurality of circuits include at least one circuit element not present in timing paths unaltered for reducing timing violations, the circuit element being inserted into the plurality of circuits based at least in part on an improvement to a first timing path of the distinct timing paths.~~

16-22. (Cancelled)

23. (Currently Amended) A The method of claim 1 further comprising making a computer readable encoding of [[a]] the semiconductor integrated circuit design, wherein the computer readable encoding is stored on a computer readable medium. ~~the computer readable encoding comprising:~~

~~one or more design file media encoding representations of a plurality of circuits having distinct timing paths, the distinct timing paths having a first common characteristic, and~~

~~wherein individual ones of the plurality of circuits include at least one circuit element not present in timing paths unaltered for reducing timing violations, the circuit element being inserted into the plurality of circuits based at least in part on an improvement to a first timing path of the distinct timing paths.~~

24-26. (Cancelled)

27. (Currently Amended) A The method of claim 1 further ~~making a semiconductor integrated circuit, the method~~ comprising:

preparing ~~the~~ one or more design files for the semiconductor integrated circuit design, ~~including a plurality of circuits having distinct timing paths, the distinct timing paths having a first common characteristic;~~

~~substituting into the plurality of circuit paths equivalent circuit elements not present in timing paths unaltered for reducing timing violations, the equivalent circuits being inserted into the same integrated circuit based at least in part on an improvement to a first timing path of the distinct timing paths; and~~

~~encoding the plurality of circuit paths in design file outputs as at least part of a computer readable media product encoding a design file representation of the semiconductor integrated circuit.~~

28-30. (Cancelled)

31. (Currently Amended) ~~A computer program product executable encoded in one or more computer readable media selected from the set of disk, tape, or other magnetic, optical, or electronic storage medium, the computer program product executable including instructions for associating a first plurality of the distinct timing paths with a first set of timing paths, individual ones of the first plurality belonging to a second set of timing paths and including a first common characteristic.~~

An article of manufacture comprising:

a computer usable medium having computer readable instructions embodied therein to cause a machine to perform operations including:

identifying distinct timing paths of the integrated circuit design, the distinct timing paths having timing violations;

identifying a first subset of the distinct timing paths including a plurality of timing paths wherein each of the plurality of timing paths includes at least one first common characteristic;

within the plurality of timing paths forming the first subset, grouping the timing paths into one or more groups, each timing path within a group having at least one second common characteristic,

correcting a first timing path violation for one of the timing paths within the group; and

repeating the first timing path violation correction for at least one of the other timing paths within the group.

32. (Currently Amended) The article of manufacture ~~computer program product executable~~, as recited in claim 31, wherein ~~the first set of timing paths is one of a first plurality of sets associated with a second set of timing paths~~ the computer readable instructions further include:

identifying a second subset of the distinct timing paths including a second plurality of timing paths.

33. (Currently Amended) The article of manufacture ~~computer program product executable~~, as recited in claim 31, wherein the second ~~first~~ common characteristic is a sequence of devices.

34. (Currently Amended) The article of manufacture ~~computer program product executable~~, as recited in claim 32, wherein each of the second plurality [[set]] of timing paths includes ~~is one of a second plurality of sets of timing paths, individual ones of the second plurality of sets of timing paths associated with~~ at least one third common characteristic.

35. (Currently Amended) The article of manufacture ~~computer program product executable~~, as recited in claim 34, wherein a particular timing path including the at least one first characteristic and the at least one third characteristic is identified with a subset based on a prioritization of the first subset and the second subset. ~~the second set of timing paths includes at least one individual timing path from a plurality of timing paths having timing violations, inclusion in the second set of timing paths based at least in part on a prioritization of individual ones of the second plurality of sets of timing paths, the individual timing path having a characteristic common to multiple ones of the second plurality of sets of timing paths.~~

36. (Currently Amended) An apparatus comprising:

means for identifying distinct timing paths of an integrated circuit design, the distinct timing paths having timing violations;

~~means for associating a first plurality of the distinct timing paths with a first set of timing paths, individual ones of the first plurality belonging to a second set of timing paths and including a first common characteristic; and~~

~~means for improving the first set of timing paths based at least in part on an improvement to an individual timing path of the first set of timing paths.~~

means for identifying a first subset of the distinct timing paths including a plurality of timing paths wherein each of the plurality of timing paths includes at least one first common characteristic;

within the plurality of timing paths forming the first subset, means for grouping the timing paths into one or more groups, each timing path within a group having at least one second common characteristic,

means for correcting a first timing path violation for one of the timing paths within the group; and

means for repeating the first timing path violation correction for at least one of the other timing paths within the group.

37. (Currently Amended) The apparatus as recited in claim 36, further comprising:

means for substituting in the integrated circuit design, a plurality of replacement circuits, each ~~individual~~ one[[s]] of the plurality of replacement circuits corresponding to a respective ~~ones of the first set of~~ timing path[[s]] of the group, the plurality of circuits based at least in part on the means for ~~improving~~ correcting a first timing path violation.

38. (New) The method of claim 1 wherein the correcting a first timing path violation comprises inserting at least one circuit element.